LHC RF Meeting 18th May 2006

Participants: Luca Arnaudon, Philippe Baudrenghien, Thomas Bohl, Olivier Brunner, Andy Butterworth, Edmond Ciapala, Frederic Dubouchet, Wolfgang Höfle, Trevor Linnecar, John Molendijk, Ragnar Olsen, Joachim Tückmantel, Daniel Valuch, Frode Weierud, Urs Wehrle.

SPECIAL TOPIC: Status of LLRF: Hardware and Software (Philippe, John and Andy)

1. Status of LLRF Modules and Hardware (John, Philippe) - See slides

LLRF VME Crates: (Michel Disdier et al.). The design is practically finalized, 5 prototypes have been delivered. We will have to organize procurement and series production of over 70 crates. For power supply and backplanes, procurement via Divisional Requests (DRs) is in progress with FI. Nine LLRF backplanes are to be received this week. The current measurement interface module is in prototype version, but preparation for production is under way.

4 Cavity Controller modules: Series production Tuner Control (25x) and Tuner Motor Controllers (in separate tuner crate) are expected soon. Tuner RF Front-end, RF feedback and clock distribution each have minor modifications, but series production will be started without further prototypes. The series analog modulator daughter-boards have been completed, but the VME carrier board remains to be done. The timing interface module will be started soon.

The RF Modulator / Klystron Polar-loop have been combined. The design still has to be done and will need testing in SM18. The Quad DDS (or Conditioning module) design has been completed and is with the design office for fabrication of the first prototype. The setpoint module design is advancing well, a number of elements needed later are included here. Digital feedback, part of the analog feedback module (one for each of I and Q), still needs to be tested in SM18 - for this the setpoint module is also needed. Due to the limited time available it is likely that the first series production run for the Switch and Protection Module will only have been tested with the switch function. Some work has to be done to specify the limiting function needed to avoid klystron saturation. The first Single Turn Feedback V1 prototype has been received. Note that this module forms the basis of the damper control loop. The first proto NIM Clock Distribution modules (4 different versions) will soon be tested. A price enquiry has been launched for 10 NIM Crates for clock distribution in the Faraday cages.

4 Synchro and Beam Control: Version 2 of the VME Trigger Unit (VTU) has been tested. The basic functionality has been tested successfully. Additions, i.e. frequency measurement and interlock system have still to be tested. Components for series production are arriving. The Wide-Band Switch and Demultiplexer prototypes will be tested soon. The injection pulse generator prototype will be tested soon. Clock Generators 560.V2 and 1128.V2 layouts are finished at Design Office. The design of the RF part of the VCXO is done and design of its VME Module has started. The Beam Phase Module RF front end is with the Design Office and the design of the digital part is ongoing. FPGA coding for the Beam Position Module has started. The Low Level Loops DSP closely follows the design of the tuner control module, but with a different input interface (design in definition) and of course specific DSP code (also in definition).

Analog/Digital Fiber-optic links: V1 of the 3 GHz link will be tested soon by PH/ESS. A lower cost link, for Frev, 40 and 400 MHz clocks is almost ready to be tested, when the Tx/Rx components arrive.

LLRF 'Infrastructure' - Faraday Cages in UX45 are progressing well. All RF cables from SR4 to UX45 are pulled. The problem of the Andrew connectors and their (partial) replacement is under urgent review. Cable lists for inter rack connections in SR4 and UX45 (ACS and ADT racks) need to be done urgently. Requests for Fiber Optic links have been made - (SR4-CCR, SR4-SPS FC, SR4-UX45), with priority on what will be needed for a sector test. Series production of special Cavity Controller patch panels with mounting of necessary RF components has been launched. The SR4 Low Level enclosure is now being actively followed up.

Milestones and Status

• UX45 Conditioning: Critical items for October are the conditioning module and the switch & protection module (see above). Important items such as the 1W pre-driver, antenna attenuator are in good shape, also the NIM clock distribution, if the V1 proto modules are successful.

• **Cavity feedback & loops tests** (2nd Phase of HW commissioning) Analog demodulator, RF modulator and Set-Point module are critical items.

• Sector Test: Critical items are the timing distributor and SPS re-phasing.

• **Beam Control:** Needed for first beam - The 1-Turn Feedback, Low Level Loops, Beam Phase and beam position modules. The damper version of the 1-Turn Feedback should obviously be tested well before first beam.

2. Status of LLRF Software (Andy) – See slides

The software structure (see diagram) has been elaborated with AB-CO. Basically the layers are: applications, middleware (CMW), then inside the front end (FE) computer: CMW server, FESA server, data store and real-time task, then the device driver.

Device drivers - The register-level hardware interface and additional "user functionality" provided by developers is included in the device access library. This is used by the FESA class or other FE software. Command-line test programs are used extensively for initial testing.

FESA classes – The device/property interface which will be used by application software. We use the most straightforward approach of having one "hardware" device class per VME module. "Virtual" device classes are also defined, linked to several hardware device classes.

Test application software - Labview applications have now been developed for tuner modules, RF feedback.

Status- Driver development is closely following hardware design: e.g. RF feedback, Tuner control, clock generator, clock distribution, analog switch and multiplexer. Work has started on the conditioning module. The software here is more complex and front-end based control applications are needed. The SM18 tests will crucial.

Next Meeting: Thursday 26th May at 08:45 in the JBA room.

E. Ciapala, 24th May 2006.