LHC RF Meeting

17th January 2008

Participants: Edmond Ciapala, Andy Butterworth, Vittorio Rossi, Eric Montesinos, Luca Arnaudon, Frode Weierud, Daniel Valuch, John Molendijk, Thomas Bohl, Maria Elena Angoletta, Joachim Tuckmantel, OlivierBrunner

1. **Status of UX45 equipment:**
   - **Conditioning progress:** Conditioning was started on Wednesday evening on Module 1 Beam 2. Three cavities successfully went through whole loop of pulse length increase. It was decided to stop the fourth cavity was due to the strange power pulse shape displayed in the conditioning program. This is being investigated by Pierre.
     Module 2 Beam 1 has not been not started yet because Line 7 had problems with crowbar firing.

   - **Vacuum gauge calibration:** It was not possible to verify the new calibration since no significant vacuum activity was seen.

   - **Software problems:** The start of conditioning was delayed due to a number of software problems:
     - The Clock Generator crate would not boot. After module and crate changes, disabling the drivers was found to solve problem. This was found to be due to an old bug in the Clock Generator module driver which had been forgotten.
     - A version change in driver generator package from CO was deployed without informing the users. Several bugs in this package meant that our drivers and FESA software no longer worked. This appears to be fixed since Wednesday.
     - At the same time, the operational software repository had been reorganised with a separate area for LHC, again without informing us, which caused some more problems.

     In total, about 4 days were potentially lost, but fortunately it was caught sufficiently early that we only lost about 1 day of conditioning.

   - **Low-Level:** The LLRF is ready for tuner tests in all 8 cavities, and RF feedback hardware is fully installed for Cavity 8 Beam 1. The clocks have been set up for Faraday Cage B, and all clock signal levels have been adjusted. This remains to be done for Faraday Cage A.

   - **Power supply (3.3V) regulation problems:** In the Cavity 8 Beam 1 feedback crate, power supply instability was found to be causing the backplane power fail detection to reboot all the FPGAs. A power supply change solved the problem. The power supply in question was one of the new version 3 modified 3.3V supplies with slowed down time constants in both the voltage and current loops. 16 of these supplies have been received, and all have now been checked. Out of the 16 supplies, 2 were found to have this fault. This will be followed up with the manufacturer. **Action: Donat, Philippe.**

   - **Function Generators:** The FGC cassettes have been installed in UX45 and SR4, and are controllable via the FIP. We can use the FGC boot program to generate test functions for the cavity setpoint.

   - **Cryo status:** There will be a cryo stop today for modifications on circuits supplying one quadrupole and the DFBs. This means isolating the D-line (He return), so the cavities cannot be powered. We should be able to restart tomorrow morning.

2. **UX45 planning**
   - It is still foreseen to warm up after week 7. For sector 34, NEG activation will continue until the end of March, so there will be no cooldown before this date. Access will be possible from week 8 to around week 11.

- With many activities now going on in parallel, Olivier has agreed to be responsible for the day-to-day coordination of the tests.

3. ADT

- **PIMs:** All Power Interlock Modules (PIMs) have been installed and tested and all except 2 are functioning correctly.

- **Transformer maintenance:** TS-EL have been contacted about the maintenance on the 2 ADT transformers. AB/PO are responsible for the maintenance, but the cost will be charged to AB/RF. The oil level needs to be checked, but the maintenance can be postponed for a few weeks. The ACS transformers were checked last year (silica gel etc.) before starting up. This was organised with S. Joffe, AB/PO.

- **Amplifier commissioning:** The 14 amplifiers have been started up and they have all reached 1A, 12kV.

4. ADT Low-Level

- The 1-turn feedback card modifications for ADT are making good progress:
  - The SerDes interface for digital data input has been successfully implemented, and impleentation of the clock management is underway.
  - Gerd has received 2 1-turn FB modules which boot with the standard 1-turn feedback firmware. The new damper-specific blocks by Gerd are to be tested using the standard 1-turn feedback code.
  - Vittorio proposes to reuse some filter blocks from SPS transverse damper.
  - The device driver from Frode can be used for these tests without major modification.
  - Results are expected in about 1 month.

Next meeting: Thursday 24th January at 08:45 in the JB Adams room 864 2 B-14.

A. Butterworth, 17th January 2008