LHC RF Meeting

15th May 2008

Participants: Vittorio Rossi, John Molendijk, Frode Weierud, Daniel Valuch, Thomas Bohl, Eric Montesinos, Wolfgang Hofle, Elena Chapochnikova, Trevor Linnecar, Andy Butterworth, Joachim Tuckmantel, Pierre Maesen, Luca Arnaudon, Olivier Brunner, Maria Elena Angoletta

1. Point 4 status and planning

- **ACS power and Faraday Cage equipment:**
  - All 16 power stations are running at 300kW. The Switch/Protection setup has been done on all lines except one which showed a strange oscillation problem with a driver amplifier.
  - A simulation of conditioning for the 8 new cavities is being done, running the conditioning program using simulated vacuum signals. This has been done for four cavities, but one has problems with power signal acquisition similar to what we have seen in the previous commissioning period (Action: Andy, Frederic). The four remaining lines will be tested in this way today.
- **Sector 3-4:** currently at 80K. The schedule is as follows:
  - Week 22: filling of the cavities
  - Week 23: low power test, zone closure and access tests
  - It should be possible to start conditioning in the first week of June.
- **Sector 4-5:** cooldown starts next week or the following week.
- **Access:** Access will not be limited in the RF zone during sector 4-5 cooldown (from next week). The same applies for ADT. Free access will be possible for 3 weeks before the start of RF tests, then we move to controlled access from the CCC.
- **Global LHC schedule:** Sector 3-4 is about 1 week late with respect to the planning, 4-5 is on schedule. The experiments are scheduled to be closed mid-July, with beam 2 weeks later.

2. Low Level progress

- **Beam phase and transverse position modules:** The series which has been delivered is not operational due to a bug in Cadence when generating the Gerber plotter files for PCB manufacture. The Design Rules Check does not correctly signal problems in the PCB layout. Some power planes were found to be shorted on the finished boards.
  - The problem is in the 10th layer of the 12 layer board, and Daniel has found it is possible to drill partially from bottom side to remove the shorts.
  - Out of the series of 20 boards, he has managed to repair 6, of which 4 boards appear to be running correctly. The VME interface appears to function, as does the gigabit serial link when connecting between modules. Daniel will check it connecting to the LL loops interface.
  - TS/DEM have some additional checks which they can run in addition to the DRC to check the Gerber file against the electrical design.
  - Daniel will continue to repair more boards and in parallel will order a new series.
- **Crate Management Module:** All components have been received, but there is no word from cabling office. The cabling of one board should be done by the end of this week or next week. John will make sure the boards are checked for layout errors as far as possible before mounting. The CMM is necessary for first beam for distribution of functions and timing on the backplane.
- **Tuning system:** The problem with the potentiometer readings is well on the way to being solved. The I^2C interface has been re-implemented by John, and is now being integrated into the overall FPGA design. Diagnostics have been added for the I^2C, and the switching of mastership between the PLC and the VME can now be done by software.
- **DSP loops module:** With the latest FPGA code the board works but the FPGA is running very hot. A problem with the VHDL code is suspected.
- **ADT DSPU:** The series is ready for mounting. Vittorio is checking one board today before cabling next week. Trevor asked if it is possible to have one card quickly for testing. Vittorio replied that it is going to an external firm so this may be impossible.

- **VCXO:** Greg has received Version 2.

- **Frequency Program DDS:** Joao is progressing with the FPGA code, and it should be ready next week. Noise measurements on this board will be crucial.

3. **Synchro system**
   - The synchro system has been successfully tested during the injection Dry Run last week. Pre-pulses and revolution frequencies are now being sent to the Beam Transfer equipment and controlled by the LHC timing and LSA application software.

4. **ADT**
   - **High voltage resistors:** Eric will visit the manufacturer next week.

5. **APW**
   - Thomas and Urs have had no time to work on LHC, but some progress has been made in the controls, with the implementation of the Mountain Range interface to OASIS which shares the acquisition hardware with the bunch length measurement.

6. **SM18**
   - **Module LHC 5:** The spare module is now fully equipped with couplers and double tubes, and is leak-tight. It is planned to put in the bunker without bakeout.
   - **Cavity Low Level:** SM18 now has fully equipped cavity controller VME crates which are currently being used for software testing.

A. Butterworth, 15th May 2008