LHC RF Meeting

3rd July 2008

Participants: John Molendijk, Frode Weierud, Daniel Valuch, Edmond Ciapala, Andy Butterworth, Vittorio Rossi, Luca Arnaudon, Eric Montesinos, Trevor Linnecar, Joachim Tuckmantel, Philippe Baudrenghien

1. Point 4 status and planning

- **Sector 3-4:** On Tuesday a chilled water failure caused loss of cooling in the Faraday cages and a mains power off due to the temperature interlock. It also caused a cryogenics failure and loss of He. The TCR have no supervision of these cooling systems, which is not acceptable, but they will have something in place in a few weeks. A patrouille was done yesterday afternoon and conditioning restarted.
  - In Module 1 Beam 1 all cavities are now at around 1MV apart from which will not go up in field; the cause of this is not fully understood. In Module 2 Beam 2 all cavities are at around 1.8MV.
  - The couplers have been conditioned at a position of 40mm, and have now all been moved to 20mm. The logging is working well, and also alarms since the new release of the LASER console.
- **Planning:** Next week we can try to carry on running in the gaps between accesses. Luca, Olivier and Pierre are away but David Landre is trained to operate the power system etc. The following week there will be continuous access.

2. SPS rephasing

- Last week the rephasing system appeared to be working perfectly in the lab. During Friday's MD, it was tested on the LHCFAST1 cycle. This showed the frequency program in the ramp to be working correctly. However, the radial steering did not work, due to a data synchronisation problem between the serial link and the DSP. John has given some help to fix this problem, reprogramming the CPLD firmware, and the radial steering now works in the lab. Problems were also encountered during the MD with timing synchronisation, and it was realised only afterwards that this was due to long latencies during the startup of the FESA software.
- Since the MD many problems have been solved and the system now works reproducibly in the lab. The total time taken to rephase is about 500ms (which is very close to the flat-top length of 500ms) but we can probably reduce this by 200ms or so. See the figure which shows the phase difference between the LHC RF and 2 x SPS RF. We can clearly see the frequency shift followed by a 100Hz amplitude coarse rephasing bump (long) and a second rephasing bump (short) followed by closure of the PLL. The gaps in between each step are due to the time taken by the ΔT measurements using the TDC in the Synchro module.

3. SPS synchro

- The SPS extraction prepulses and warnings will in future be generated using new LHC-style injection pulse generator modules to generate extraction pulses in SPS. This system will be installed in parallel with the existing hardware. Work is in progress (Greg/Frederic).

4. Low Level RF

- **FPGA clock level adaptation:** The modification has been done on the RF Modulator and Setpoint modules, and the cards are ready to be re-installed. The modifications have not been done for the Tuner modules as these are currently being used for conditioning. This could be done in weeks 28/29.
- **Test setup for Beam Control:** The synchro loop has been closed. Jorge is now back from exams. There is an excessive thermal drift in the VCXO, and this is now being tested in an oven by Greg. 5 degrees Celsius gives a frequency offset of about 1kHz at 400MHz.
- **Beam phase:** The FPGA firmware is almost finished, but Daniel has to juggle priorities. All series production has been received, and the next step is testing with both digital and analogue cards together.

- **Dual Frequency Program:** This is progressing but is not finished yet. The frequency change during ramp looks OK, but the output is somewhat noisy. In any case, the DDS output has very poor spectral purity as the output frequency of 100MHz is generated using a 500MHz clock, i.e. only 5 steps per cycle.
- **Tuner control:** New firmware and DSP code installed everywhere in sector 3-4. John and Maria Elena have tested flashing the DSP ROM through backplane JTAG. Frederic is working on software to load via Crate Management Module.
- **Crate Management Module:** The series should be received towards the end of July.
- **Beam out timing distribution:** Version 1 of the NIM module has been tested and is going for production.
- **Function Generators:** The Low Level Loops and Dual Frequency Program modules consume lots of functions. The function transmission functions correctly but about once every 10 seconds one 1ms frame is lost for several channels. At the moment it is not known whether the problem is in the FGC distributer or in VME modules. This problem should be solved eventually but it is not catastrophic if we lose data during one millisecond from time to time. Fortunately the PO group have equipped the FGC with very good diagnostics including counts of lost frames etc.

5. ADT

- **Power tests** are ongoing. There are enough spare HV resistors for 2 amplifiers.
- **Controls tests** are progressing; the second part of the slow control FESA class was implemented by David before leaving on holiday. There are some minor problems, Fred and Luca will try to fix these today, otherwise we wait for David to return. The logging and alarms are working well.
- **Access system:** All access interlocks have been tested, and we have the green light from Ghislain Roy to switch on.
    - When an access interlock occurs, the RF switches off before the 18kV. It is possible to switch on the 18kV remotely from the CCC (only after an access interlock).
    - Wolfgang will need to have access with the 18kV and ADT on.

6. ADT Low Level

- **ADT DSPU:** All 4 pre-series modules work without problem. One had a problem with power supply capacitors due to overheating during lead-free reflow. Also apparently non-elastic deformations on the card can cause solder joint breaking, which is a general problem with the lead-free soldering process.
  Clock management and the SerDes fast serial links have been tested with a loopback to the same card; the next step is to test between the DSPU and the front-end card (with Gerd).

7. US-LARP

- Dan van Winkle and Claudio Rivetta have returned to SLAC. They have made good progress with their Matlab software which is now working quite well. The first objective is to be able to measure the RF feedback open-loop response and adjust the relative phase of the digital and analogue feedbacks. They will continue to work remotely from SLAC and will come back in August/September for tests on live cavities.

A. Butterworth, 6th July 2008