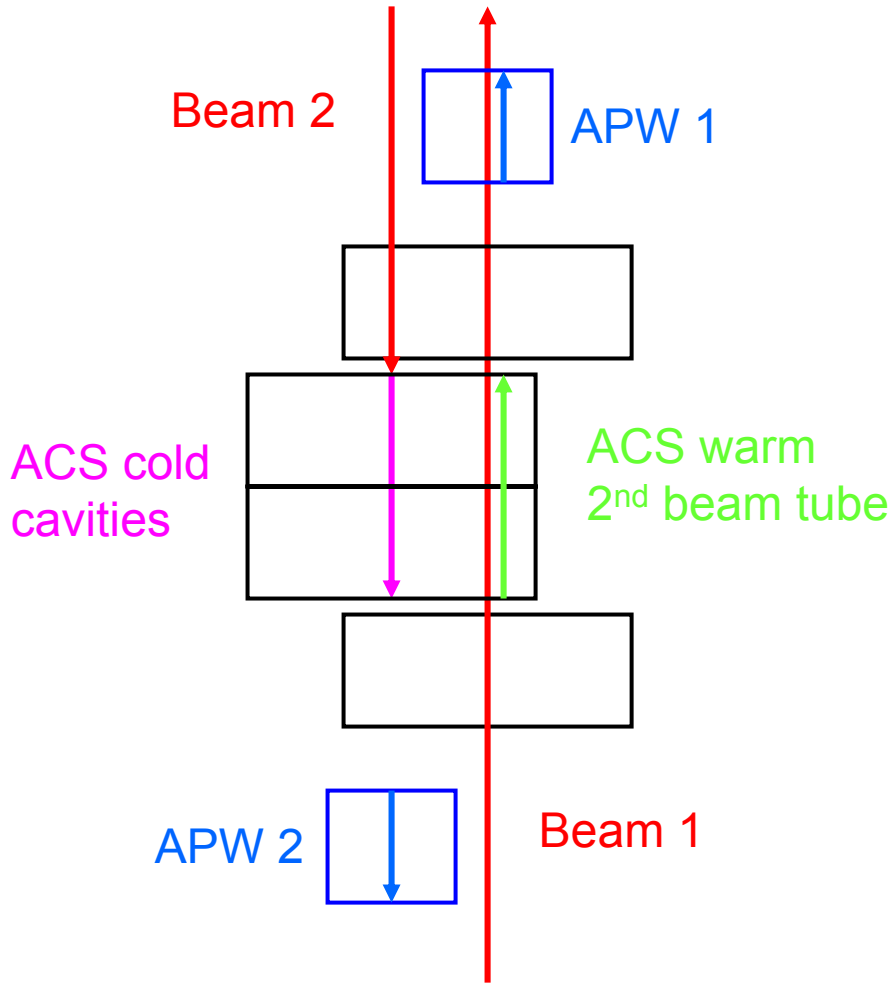
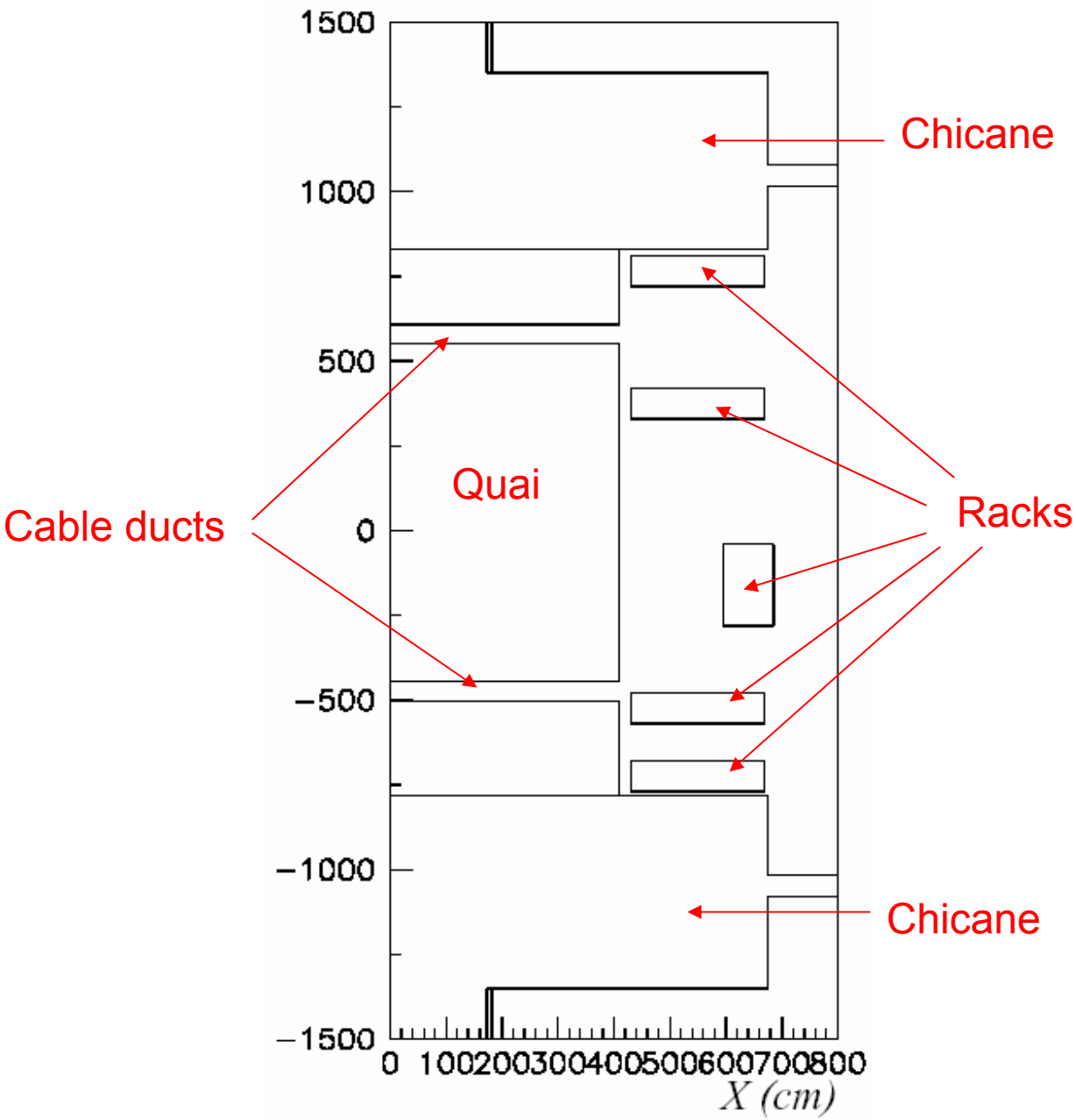
Source regions for different simulations

Simulation	Source region
Beam 1	Whole straight section Uniform vacuum 4 x 10^{-12} mbar @ 300K
Beam2	Incoming half of straight section, ending at ACS modules Uniform vacuum 4 x 10^{-12} mbar @ 300K
ACS cold cavities	ACS modules 2 and 3 Vacuum 1 x 10^{-10} mbar @ 4K
ACS warm 2nd beam tube	ACS modules 2 and 3 Vacuum 1 x 10^{-10} mbar @ 300K
APW 1	APW 1 Vacuum 1 x 10^{-7} mbar @ 300K
APW 2	APW 1 Vacuum 1 x 10^{-7} mbar @ 300K



Geometry for result plots

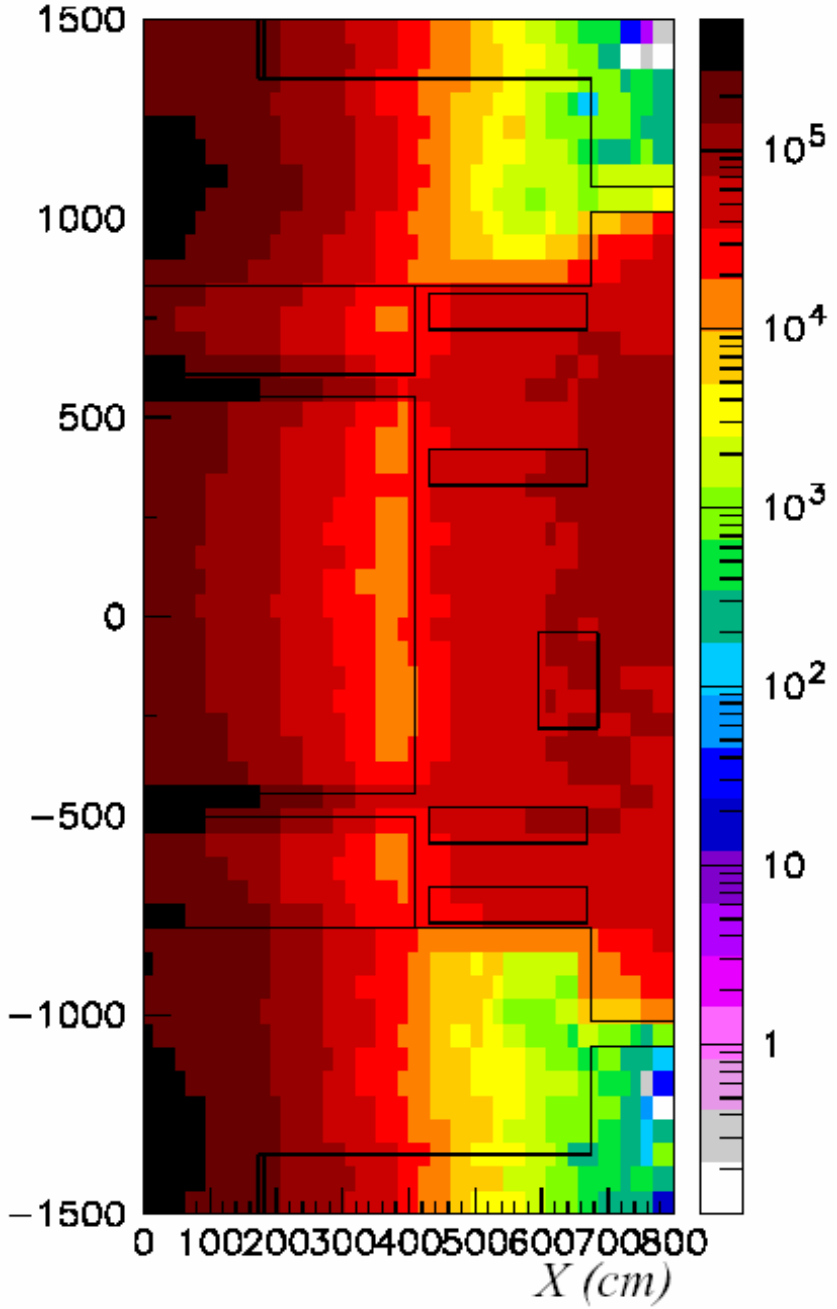


Scoring:

- On 3D mesh throughout whole geometry:
  - Total ionising dose
  - total particle fluence
  - fluence normalised to 1 MeV equivalent displacement damage in silicon
- In racks:
  - Energy spectra of all particles

Warm beam tube, beam from top

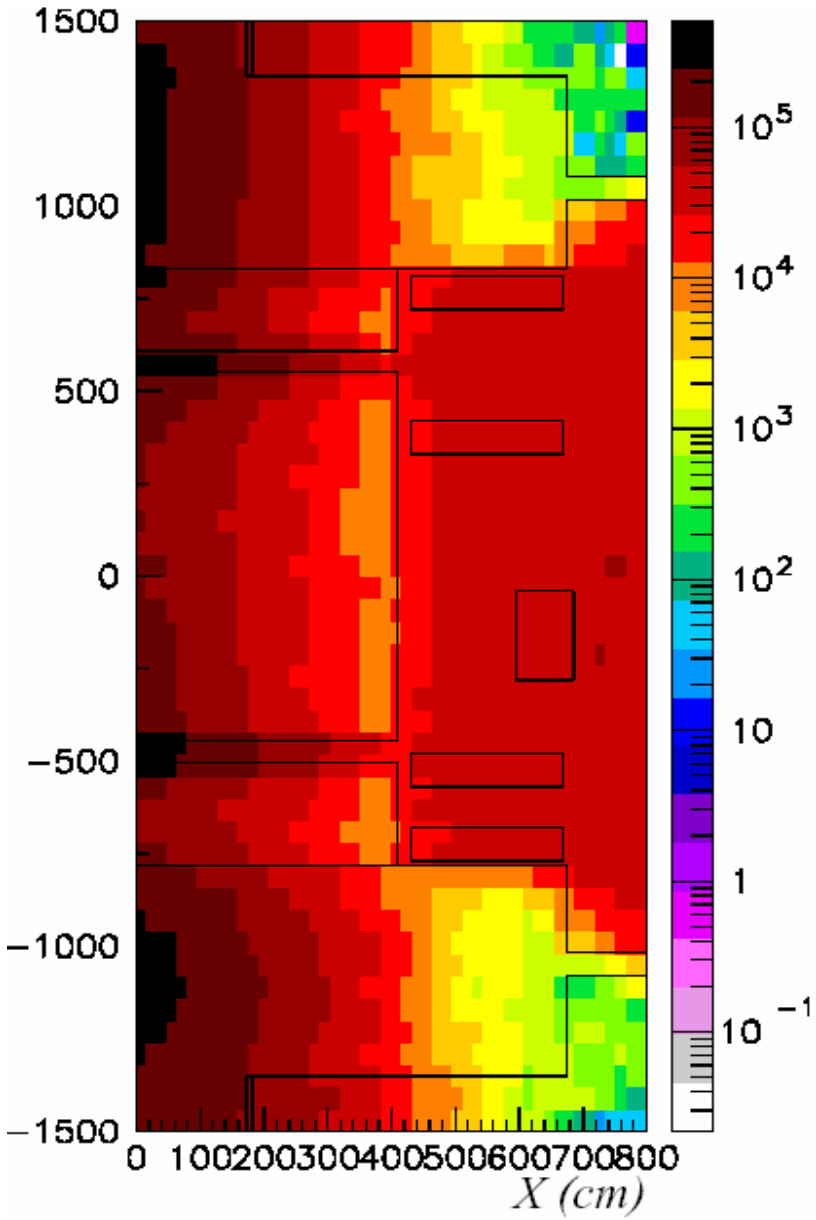
50% CH_4 50% H_2
4 x 10^{-12} mbar
300 K



Fluence normalised to 1 MeV equivalent displacement damage (cm^{-2} $year^{-1}$)

Warm beam tube, beam from bottom

50% CH_4 50% H_2
4 x 10^{-12} mbar
300 K



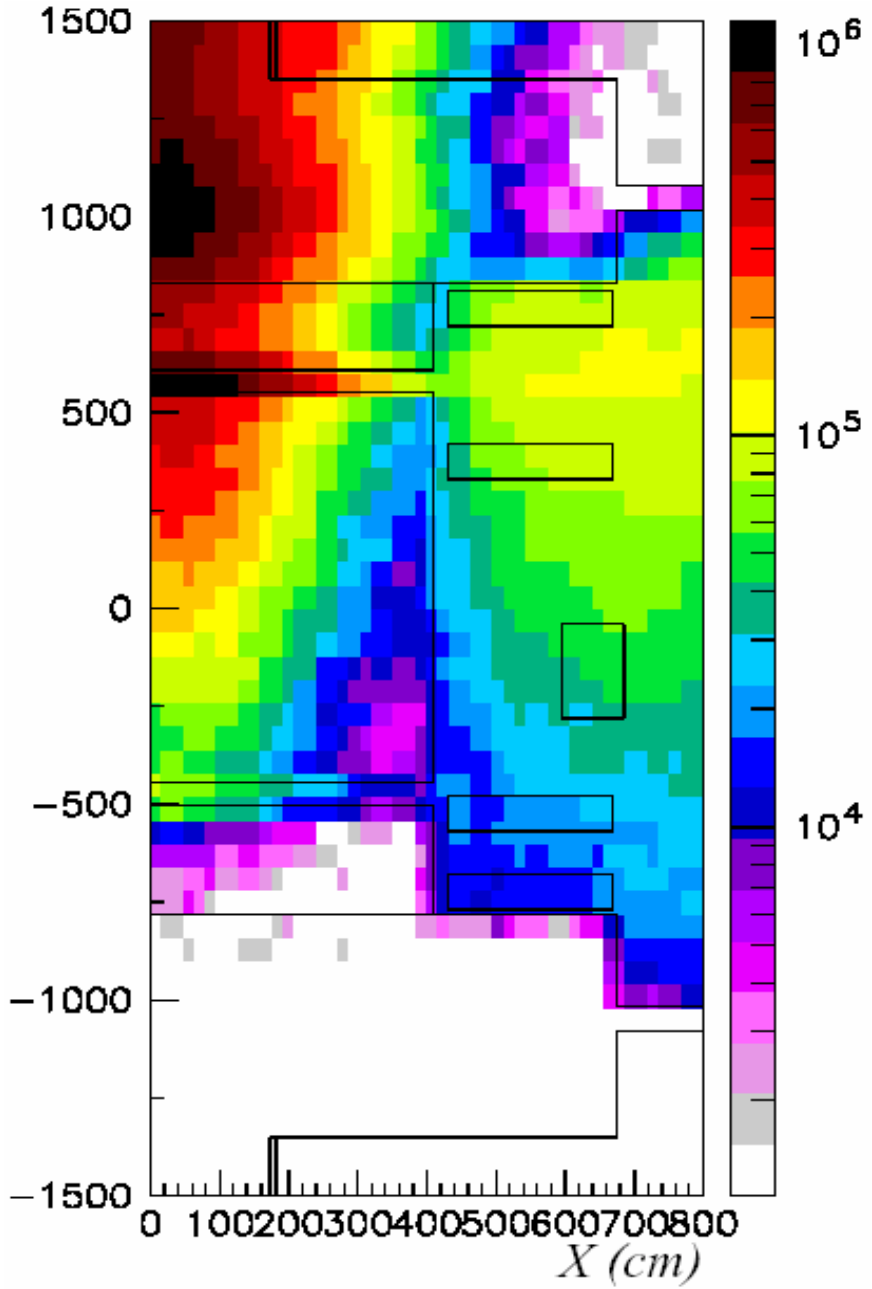
Fluence normalised to 1 MeV equivalent displacement damage (cm^{-2} $year^{-1}$)

Averaged over vertical dimension of racks

ACS warm 2nd beam tube, beam from bottom

100% CH_4
1 x 10^{-10} mbar
300 K

Too pessimistic?



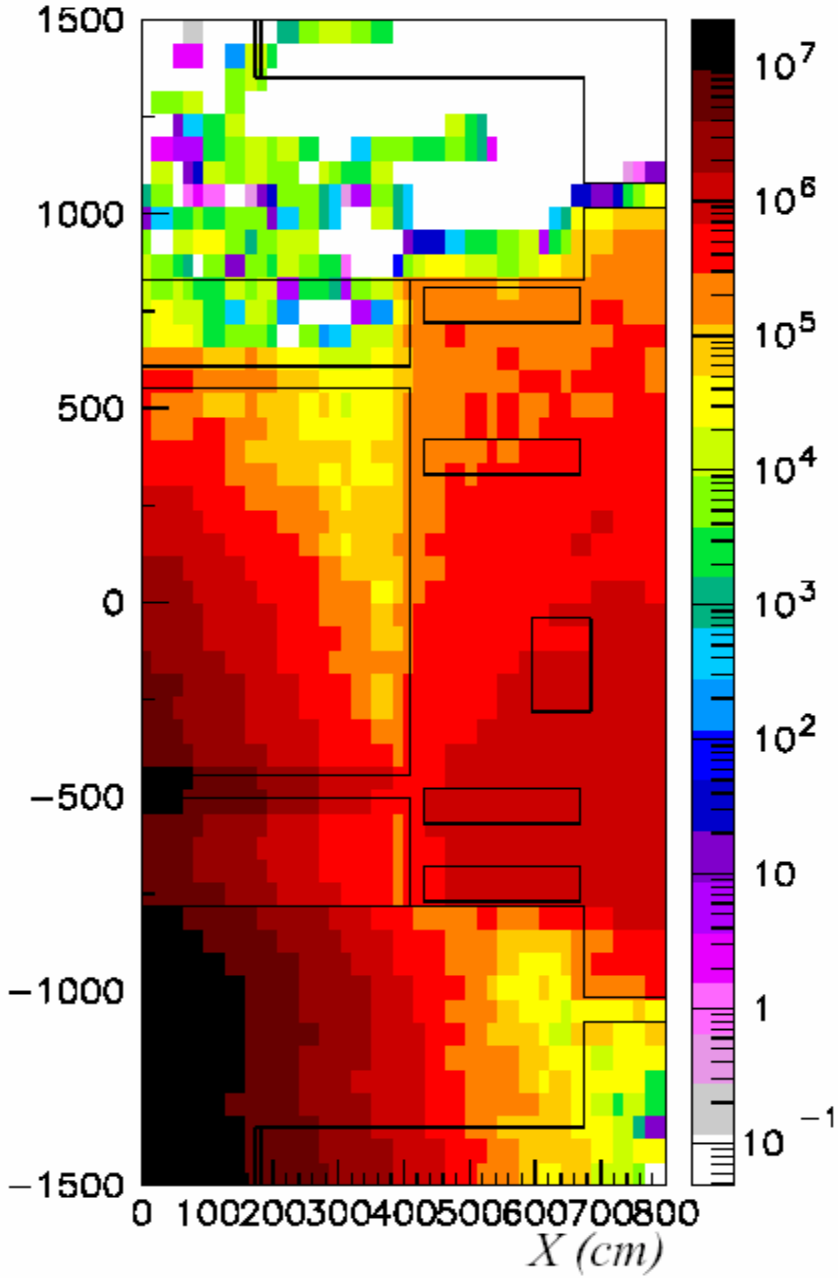
Fluence normalised to 1 MeV equivalent displacement damage (cm^{-2} $year^{-1}$)

Averaged over vertical dimension of racks

ACS cold cavities, beam from top

90% H_2 10% CO
1 x 10^{-10} mbar
4 K

Too pessimistic?



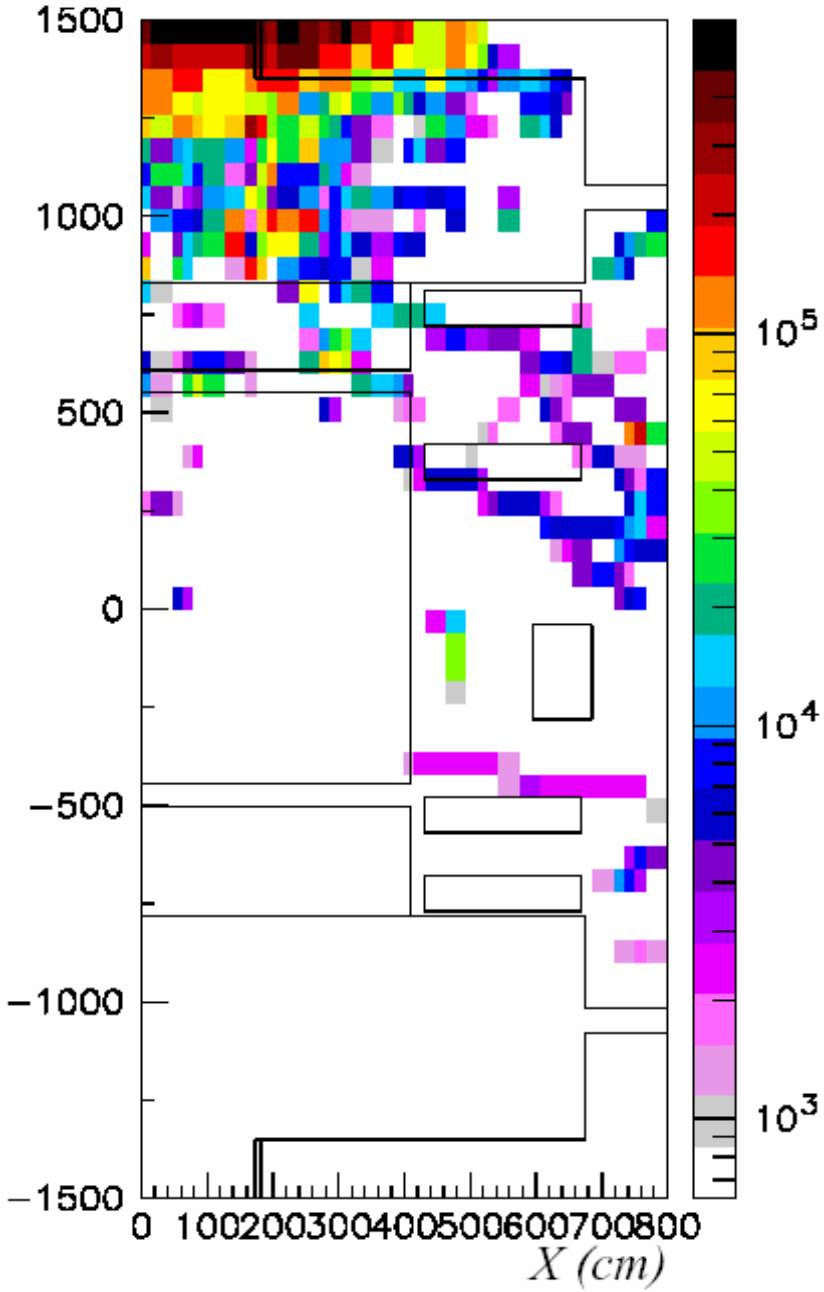
Fluence normalised to 1 MeV equivalent displacement damage (cm^{-2} $year^{-1}$)

Averaged over vertical dimension of racks

APW 1, beam from bottom

40% H_2 30% CO
25% H_2O 5% CO_2
1 x 10^{-7} mbar
300 K

Pessimistic?



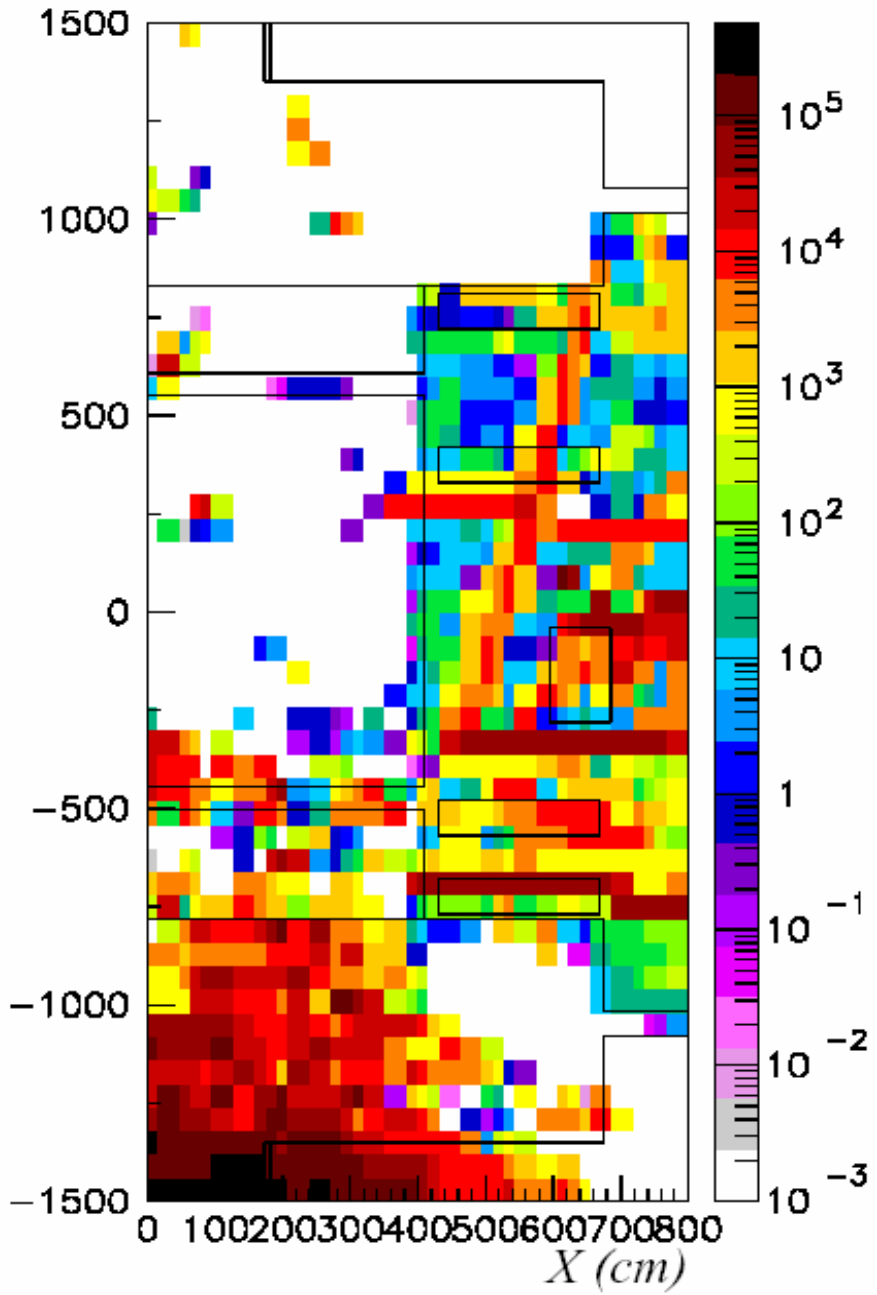
Fluence normalised to 1 MeV equivalent displacement damage (cm^{-2} $year^{-1}$)

Averaged over vertical dimension of racks

APW 2, beam from top

40% H_2 30% CO
25% H_2O 5% CO_2
1 x 10^{-7} mbar
300 K

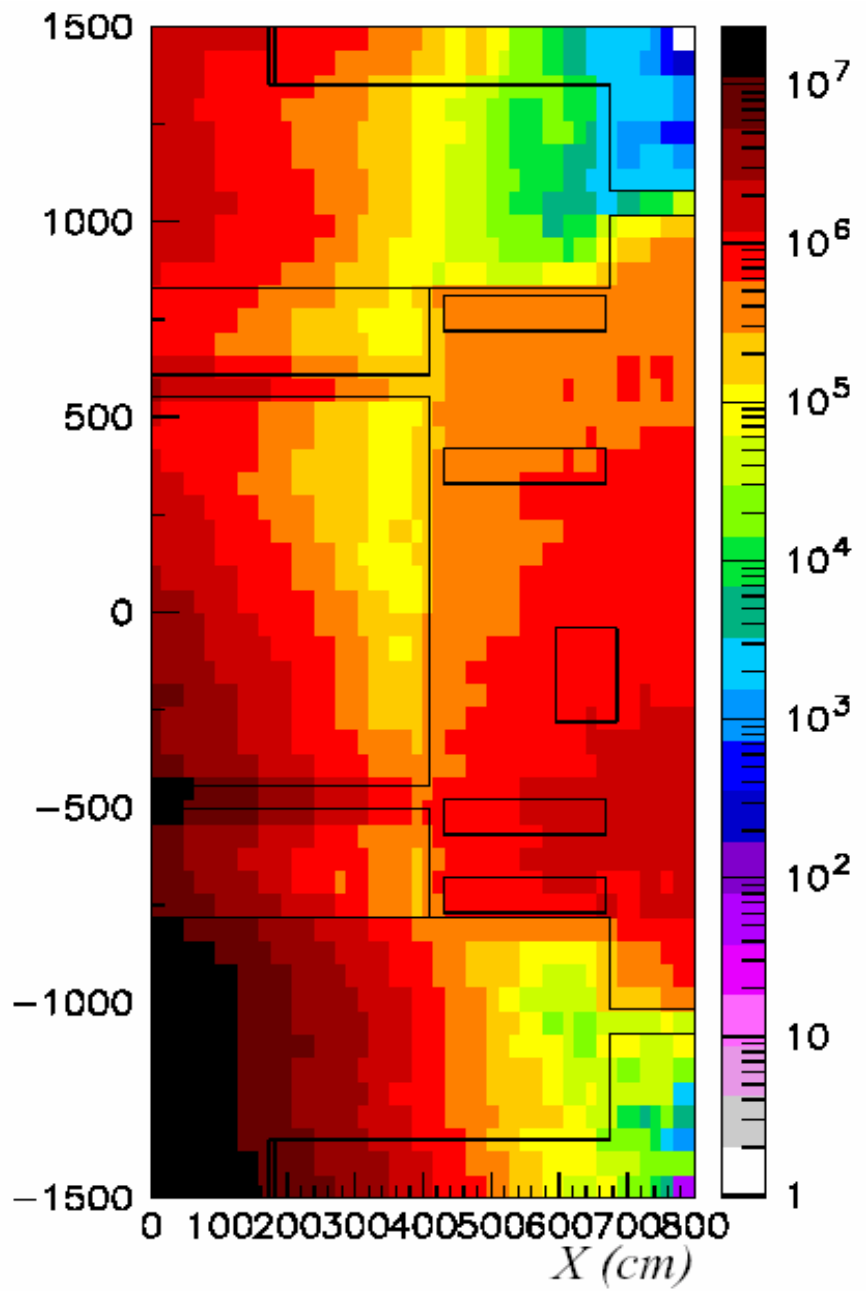
Pessimistic?



Fluence normalised to 1 MeV equivalent displacement damage (cm^{-2} $year^{-1}$)

Averaged over vertical dimension of racks

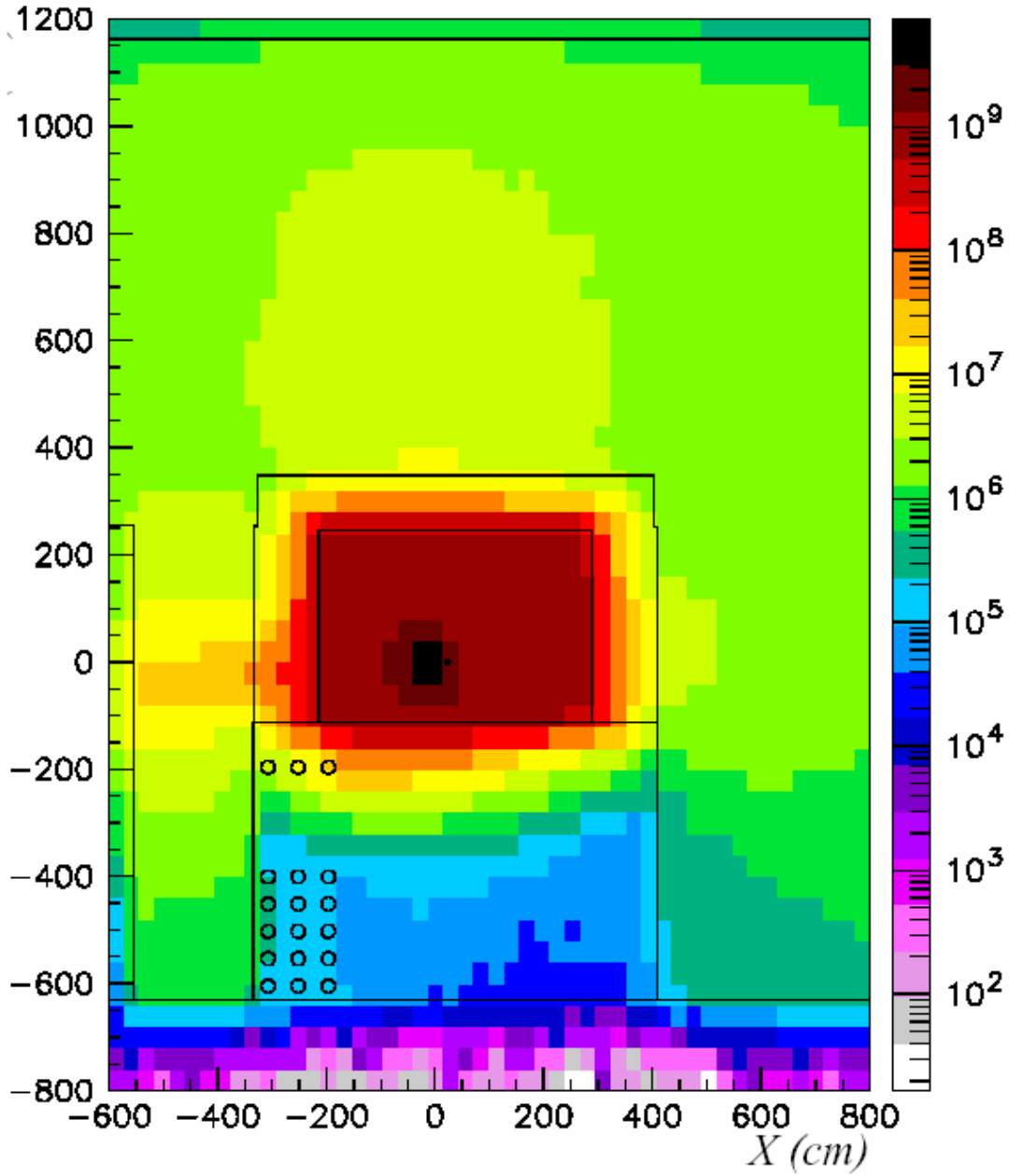
Sum of all simulations



Fluence normalised to 1 MeV equivalent displacement damage (cm^{-2} $year^{-1}$)

Averaged over vertical dimension of racks

Sum of all simulations – vertical view



Fluence normalised to 1 MeV equivalent displacement damage (cm^{-2} $year^{-1}$)

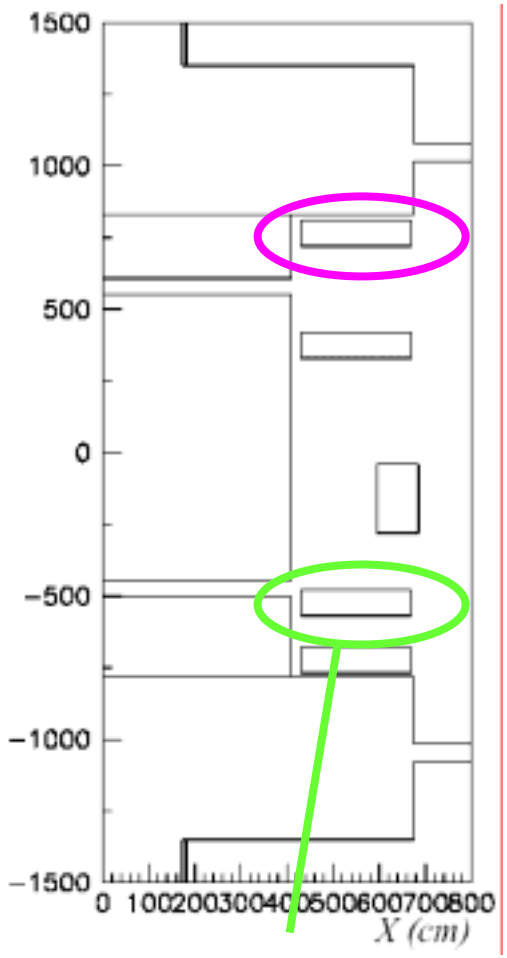
Averaged over horizontal dimension of rack platform

Estimated particle fluence at the racks

- Some simulations missing, so
  - scoring in rack
  - added in scores for “ACS warm” and “ACS cold” from rack

Total fluence > 20 MeV of	cm^{-2} y^{-1}	%
all particles	3.7E+05	100
neutrons	3.5E+05	95.1
protons	7.6E+03	2.1
pions	1.6E+01	0.004
muons	1.8E+03	0.49

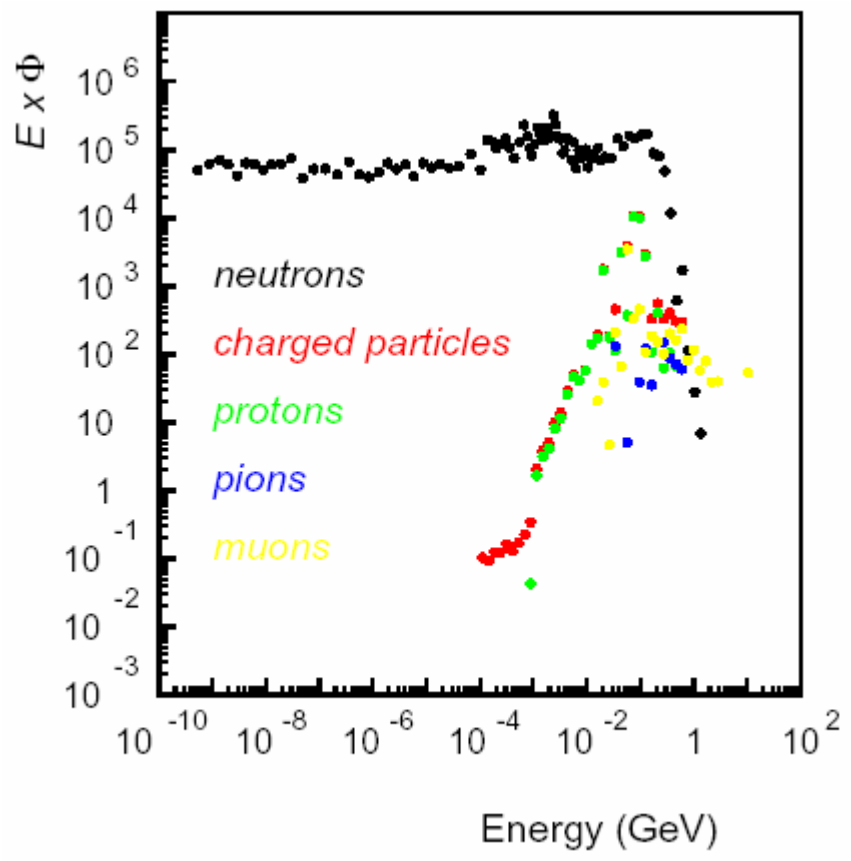
Disclaimer:
“The simulation numbers are to indicate an order of magnitude of the estimated risk but it is not the reality. Perhaps you should stress this in your talk...
You have to define a safety factor to these numbers that will include all the missing sources and the ‘error’ that we might make because of various reasons”



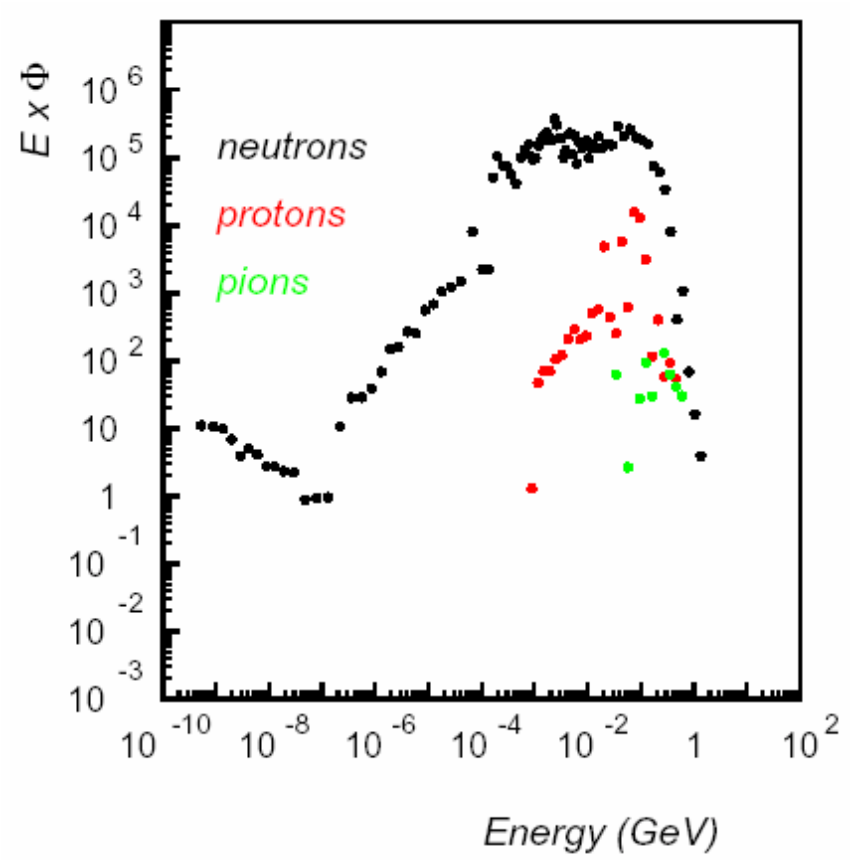
Scoring in racks volume (with some corrections)

Particle energy spectra at the racks

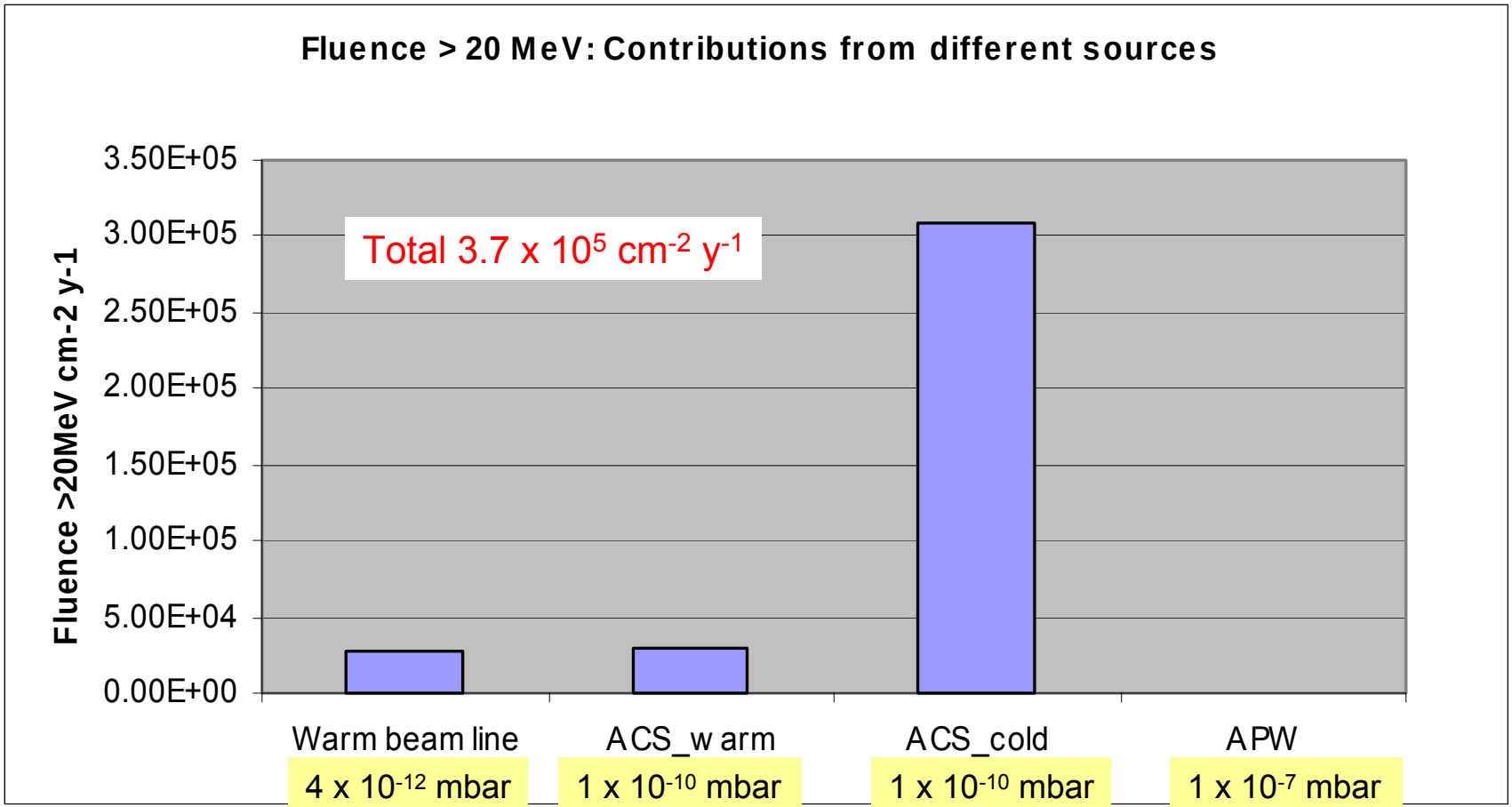
Raw particle fluence spectra



Normalised to 1 MeV equivalent displacement damage



Contribution from different source regions



- Fluence contribution scales linearly with vacuum
  - Reducing from 10^{-10} → 10^{-11} would bring total to $<10^4$ cm^{-2} y^{-1}

Single Event Upset cross-sections

Xilinx SRAM-based XC4036XLA FPGA

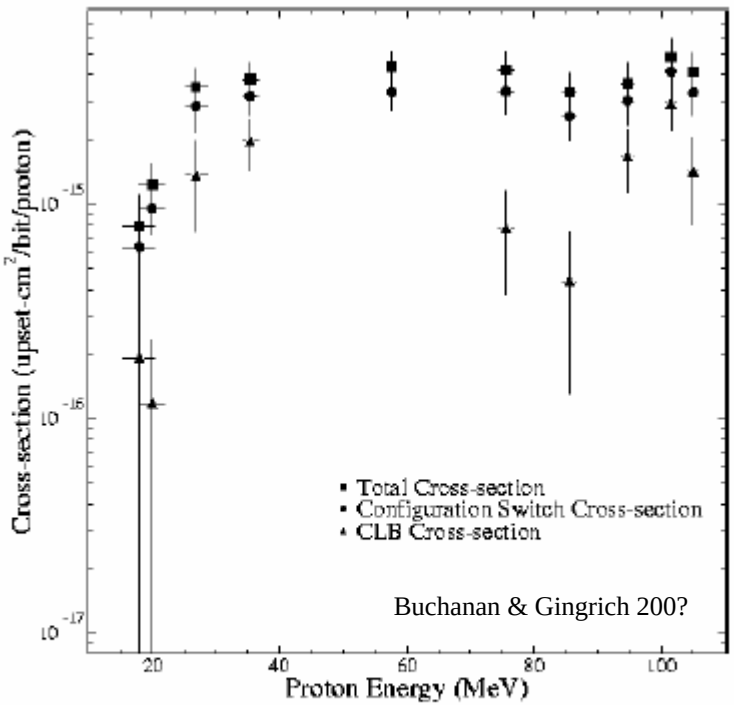
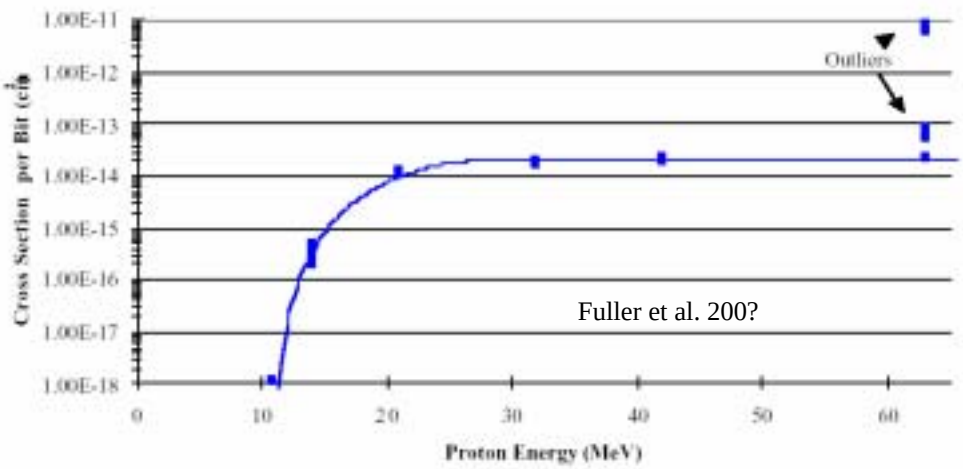


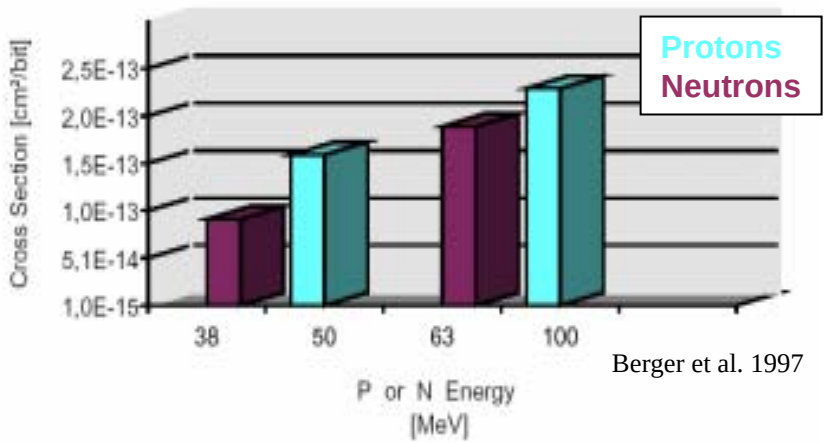
Figure 6: The SEU cross-sections for the total device, configuration logic blocks, and configuration switches normalized by the number of bits. The CLB upset cross-section at 57.7 MeV, with no measured upsets, has been omitted.

Proton SEU Cross Section for the Xilinx Virtex XQVR300

(Radiation hardened FPGA)



Hitachi HM628512P 512K x 8 SRAM



Single Event Upset cross-sections (contd)

Cross-section typically ~10^{-13} cm^2 per bit

(between 10^{-15} and 10^{-12} depending on exact device design)

→ for a fluence of 3.7 x 10^5 $cm^{-2}y^{-1}$ we expect ~3.7 x 10^{-8} errors per year per bit

Xilinx devices have ~6 SRAM bits per logic cell → 12 M bits for 2 M gates

→ we would expect ~0.4 bit errors per device per year

but don't forget the margin of error

XILINX claim that "Only a Small Percentage of SEUs Actually Causes a Logic Error"

"Extensive research indicates that somewhere between 1 in 10 to 1 in 40 configuration cells actually affect any given design, which means that 90% to 97% of the configuration latches in any given application are "don't care" "

→ Measurements!

Tentative conclusions

- Some simulations are missing, but we can already make a reasonable estimate of particle fluences from the data we have

- From the simulation results we expect a 2M gate FPGA to suffer about 0.4 single event upsets to its configuration memory per year
  - neutron SEU cross-section for the FPGA devices we are using could be +/- an order of magnitude
  - this is without a margin of error on the simulation results → 1 order of magnitude
  - true failure rate depends on the application
  - do some radiation tests when we have some hardware
  - don't forget other devices and equipment e.g. Power PC computers

- The results depend strongly on the vacuum quality in the cavities
  - assumed 10^{-10} which is probably too pessimistic
  - reducing to 10^{-11} would reduce the fluence by a factor of ~6

- Effects of poor vacuum in APW
  - not a problem if APWs placed on the downstream side